

GARY P. MORRISON ET AL.

Serial No. 10/034,827 (TI-31373)

Filed December 26, 2001 (As noted in Petition)

For: CHIP-SCALE PACKAGES STACKED ON FOLDED INTERCONNECTOR FOR VERTICAL ASSEMBLY ON SUBSTRATES

Art Unit 2827

Examiner James M. Mitchell

Customer No. 23494

Director of the United States Patent and Trademark Office P. O. Box 1450 Alexandria, VA 22313-1450 CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that the attached document is being deposited with the United States Postal Service with sufficient postage for First Class Mail in an envelope addressed to Director of the United States Patent and Trademark Office, P.O. Box 1450,, Alexandria, VA 22313-1450 or is being facsimile transmitted on the date indicated below:

Jav M. Cantor, Reg. No. 19,906

Sir:

DECLARATION UNDER 37 C.F.R. 1.132

Jay M. Cantor declares as follows:

Applicants, through their attorney, hereby submit that they invented or discovered the claimed subject matter of the subject application and that it was "ready for patenting" in accordance with the requirements of 35 U.S.C. 102 prior to the effective date of the cited Japanese publication number 2001-217338, published October 10, 2001 according to the Patent Abstracts of Japan.

The attached invention disclosure was submitted to the Patent Department of the assignee, Texas Instruments Incorporated prior to October 8, 2001. Also, the provisional application Serial No.60/258,525, filed December 28, 2000 for which priority was not

granted in the subject application also provides proof that the invention as claimed in the subject application was "ready for patenting" prior to the publication date of the above noted Japanese publication.

In accordance with the decision by the United States Supreme Court in <u>Pfaff v</u> <u>Wells Electronics</u>, 525 U.S. 55 (U.S. 1998), the meaning of the term "invention" was specifically defined as it applies to 35 U.S.C.

It is clear from reading 35 U.S.C. that the word "invention" in the statute "does not contain any express requirement that an invention must be reduced to practice" as stated in Pfaff and even in section 102(g) where the conception and reduction to practice are specifically mentioned, there is no requirement that these be the only factors If follows, first, that 35 U.S.C. nowhere defines "invention" by a considered. determination solely of the questions of reduction to practice or conception with diligence up to a reduction to practice (actual or constructive). While a proper showing of a reduction to practice or conception with diligence up to a reduction to practice does establish invention under 35 U.S.C, there is nothing in 35 U.S.C. which limits the definition of invention to only those factors. This is confirmed in Pfaff wherein the Court rejected the longstanding precedent set forth above by stating [III] "Pfaff nevertheless argues that longstanding precedent buttressed by the strong interest in providing inventors with a clear standard identifying the onset of the 1-year period, justifies a special interpretation of the word 'invention' as used in § 102(b). We are persuaded that this nontextual argument should be rejected."

As stated in the opinion in defining the term "invention", the Court states that "Thus petitioner's argument calls into question the standard applied by the Court of

Appeals, but it does not persuade us that it is necessary to engraft a reduction to practice element into the meaning of the term 'invention' as used in § 102(b)."

The Court further states:

"The word 'invention' must refer to a concept that is complete, rather than merely one that is 'substantially complete.' It is true that reduction to practice ordinarily provides the best evidence that an invention is complete. But just because reduction to practice is sufficient evidence of completion, it does not follow that proof of reduction to practice is necessary in every case. Indeed, both the facts of the Telephone Cases and the facts of this case demonstrate that one can prove that an invention is complete and ready for patenting before it has actually been reduced to practice."

The Court concluded that the on-sale bar applies when two conditions are satisfied, the first condition not being applicable in this case because it relates to conditions of sale. However, the second condition relates to the definition of "invention" and states:

"Second, the invention must be ready for patenting. That condition may be satisfied in at least two ways: by proof of reduction to practice before the critical date; or by proof that prior to the critical date the inventor had prepared drawing or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention. In this case the second condition of the on-sale bar is satisfied because the drawing Pfaff sent to the manufacturer before the critical date fully disclosed the invention" (underline not in original)

It follows that an invention disclosure is provided which contains "prepared drawing or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention".

In the present case, the attached disclosure form contains the claimed subject matter of the subject application as does the provisional application referred to above. It follows that the attached form and the provisional application contain a disclosure which was ready for patenting as defined by the Supreme Court in Pfaff and that appellant is entitled to rely at least upon the date of submission of the attached disclosure form to the assignee patent department. (and possibly an earlier date if it can be established) as well as the filing date of the above referenced provisional application.

The undersigned states, on information and belief and under penalty of perjury, that the attached disclosure form was submitted to the Texas Instruments patent department prior to October 8, 2001 and that the invention is that of the applicants as attested to by their signatures on the declaration filed with the subject application.

Respectfully submitted,

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Jay M. Cantor

Attorney for Applicant(s)

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What are the advantages of your solution?

Offers a very low cost solution.

qualified MicroStar BGA packaging extensively.

MicroStar BGAs to our major customers with great success.

OSURE FORM	
	DOCKET NO. TI $3/3$

+ TE ELECTRONICALLY TRANSMITTE	D, PROCESSING OF YOUR DISCLOSURE *
* CANNOT BE COMPLETED WITHOUT	A FOLLOW-UP COPY SIGNED AND *
* DATED BY ALL INVENTORS AND A	T LEAST ONE WITNESS. *
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Please suggest a descriptive titl	e for your invention:
A low cost, stacked multi-chip p	ackage using existing MicroStar BGA/Jr
package and assembly technology.	
This invention supports strategy:	(check 1 or more)
() DRAM DSPS	•
\	(x) Wireless
() DLP () Materials	(x) Video
() Fab/Processes	(x) Set Top
(x) Assembly/Test/Packaging	(x) Application Specific
() Other	(x) Remote/Access/Networking
• • • • • • • • • • • • • • • • • • • •	(x) Emerging Markets
	(x) Mixed Signal & Logic
	(x) Mass Storage
	() Other
What is the problem solved by you	ir invention?
Cost - in development, tooling ar	nd manufacturing. Stacked multi-chip
nackaging is expensive to develor	o, implement and yield, although it offers
the advantages of saving board sp	pace and improving performance and
functionality.	
	-12
What is your solution to the prob	ry low cost packaging technology —
Innovative use of an existing ve	ible substrate material, these packages
migrostar BGA/UF. With its ilea	low cost, interconnected, stacked multi-
chin packaging solutions By usi	ng available thin versions of the
MigroStar BCA/JR package, the st	ack height can be kept within acceptable
limits for many applications. Se	e the attached diagrams.
When was your solution first cond	ceptually or mentally
complete? Date: _//	
What is the first tangible eviden	nce of such completion?
Date://	 •
What is different about your solu	ution, compared with other solutions to the
same problem?	ector, compared with other obtained to the
This concept uses an existing lo	w cost, reliable technology, infra-
structure, materials, equipment,	process and tooling.

• Proven technology and reliability. TI has developed, characterized and

• Based on an industry-preferred package. TI has shipped over 200 million

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 No significant additional tooling or development costs.
What TI products, processes, projects or operations currently implement your invention? None.
10. What is the date of the first implementation? TBD
11. What record exists to prove this date? TBD
12. Is there any future implementation planned? (Y/N) Y If so, please furnish the TI PART No. or project name: TBD
13. Has the invention been published or disclosed to anyone outside of TI? (Y/N) N When? If planned - when? (Catalog, advertising, data book, application note, conference paper, magazine article, TI TJ, proposal document.) Was there a nondisclosure agreement (NDA)? (Y/N)
14. Has a TI product incorporating the invention been publicly introduced, quoted, sampled or shipped? (Y/N)_N When? If plannedwhen?
15. Was the invention conceived or first implemented in the performance of a government contract or subcontract? (Y/N) N Contract #:
THE INVENTION DESCRIBED BY THIS DISCLOSURE IS SUBMITTED PURSUANT TO MY EMPLOYMENT AGREEMENT WITH TEXAS INSTRUMENTS INCORPORATED OR A TI SUBSIDIARY (SPECIFY): Has this disclosure been previously sent to the Patent Department electronically (unsigned)? (Y/N) N
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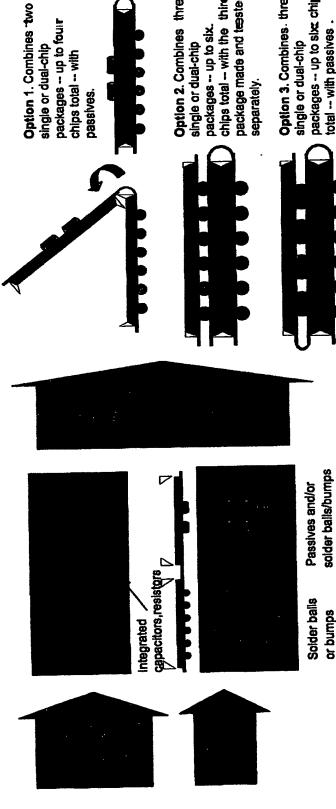
Employee #:	II Divison & Cost Cent	er <u>03</u> - 2050
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Employee #: 66802/ TI Division &	Cost Center <u>03</u> - 1	<u> </u>
Phone #: Country of	Citizenship:	
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This invention disclosure with an understood by me on//	y attachments was re 	ead and
Witness 1:	Date	
This invention disclosure with an understood by me on//		d and
Witness 2:	Date	
***********END OF	FORM*********	

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chip Packaging with MicroStar BGA/Jr Technology MultiStar BGA -- Very Low Cost, Stacked Multi-



Option 2. Combines three package made and tested chips total -- with the third packages -- up to six. single or dual-chip

packages -- up to six chips Option 3. Combines. three single or dual-chip

total -- with passives

Option 4. Combines: three packages -- up to six single or dual-chip chips total.

Matched sets of packages, each package may be

single or dual-chip.

The chips may be interconnected by substrate traces and/or solder balls and passives.



· Integrated capacitors or resistors may be used in

the folded tape area.

N. 12.16

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Conventional passive components may be included to improve performance.

different combinations Other options. Marny are possible.

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